

## 阵列基板铜工艺不良研究

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## Cu defects in array process

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**Abstract:** The mechanism of defects on Cu process along with the development of new product is studied in this paper, and improvement methods are proposed. The results show that the high flow of  $O_2$  used in post ashing corrodes the Cu in PVX1 (The First passivation Layer) etch, and makes the Cu hole blackened. After adding the  $H_2$  treatment step, CuO can be reduced to Cu, and the hole appears metallic white color during CD (Critical Dimension) measurement. During 1ITO (The First Indium Tin Oxides Layer) etch process, high temperature annealing results in the occurrence of serious oxidation of exposed SD Cu. Skipping anneal or changing mask design can avoid the defect. In the VIA etch step, high content of  $O_2$  oxidizes the Cu, resulting in the break of conduction between gate and SD through the hole which leads to the occurrence of vertical line Mura. Reducing the content of  $O_2$  of VIA etch can solve the problem.

**Key words:** array process; Cu corrosion; Cu oxidation; black hole defect; anneal; vertical line Mura

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**摘要:** 本文结合产品开发过程中遇到的铜相关不良现象进行研究, 提出了有效的改善措施。结果表明, 在第一次氮化硅刻蚀中的后灰化工序有高含量的氧气, 会使过孔内部铜发生氧化而发黑。使用氢等离子体处理, 可以将氧化铜还原成铜, 在生产线上光学设备测量时过孔反射出金属白色。在氧化铜锡刻蚀过程中, 高温退火会造成裸露的铜发生严重氧化, 需要去掉退火步骤或者更改设计来规避。在第二次氮化硅刻蚀步骤中, 高含量的氧会氧化过孔处的铜, 造成过孔连接异常, 降低刻蚀步骤中氧气含量可以解决该不良。

**关键词:** 阵列工艺; 铜腐蚀; 铜氧化; 黑孔不良; 退火; 垂直黑线不良

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### 1 Introduction

Driven by the high refresh rate and high

resolution of display products, many display plants use low resistivity Cu instead of Al in the gate or SD layer, even in both layers at the same time, so as to avoid the risk of resistor-capaci-

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tance delay<sup>[1-3]</sup>. ORG (Organic) film material have many advantages such as low dielectric constant and high flatness which make it widely used in TFT-LCD<sup>[4]</sup>. when converting Al to Cu, not only the DEP (Deposition) process changes, but also mask, etch and strip processes have to change correspondingly. So the process becomes more complicated when ORG is added. In this paper, according to a HADS (High Advanced Dimension Switch) mode product with organic film development process, the defects caused by the use of Cu materials are studied and improvement methods are also given to solve the technological challenges.

## 2 Array Process and Defects

As shown in Fig. 1, a typical array process of 6 mask product is described. The gate layer is firstly fabricated. Then active and SD film are deposited successively and HTM (Half Tone Mask) is used for once exposure which needs twice wet etch, twice dry etch and once ashing processes, thus presenting TFT channel structure. Finally, ORG/1ITO/VIA/2ITO (The Second ITO Layer) layers are made. The thickness of Cu in gate and SD layers are both 300 nm.

Fig. 2 is taken on ORG FICD (Final Inspection Critical Dimension) in AA (Active Area) zone. It can be seen that the pixel hole is very

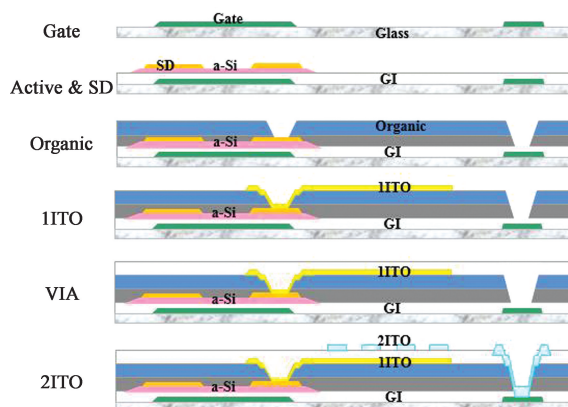


Fig.1 Schematic diagram of organic film product structure

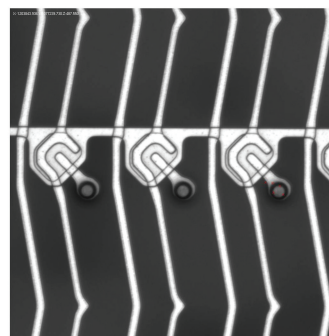


Fig.2 Defect of pixel hole in AA zone

black. This color is abnormal because the inside of the hole is copper and it should be as bright white as the SD line under the same vision.

As shown in Fig. 3, GOA (Gate on Array) hole is taken by optical microscope after the array substrate is fabricated. Black stain and abnormal color can be observed in the left SD hole while the gate hole on the right is clean.

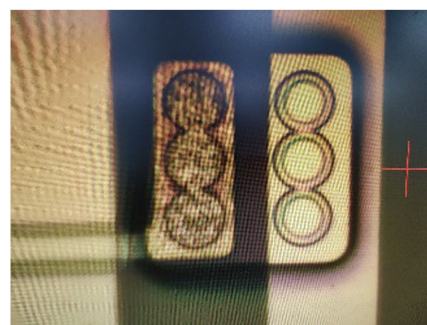


Fig.3 Defect of SD hole in GOA zone

From Fig. 4, we can see that vertical black line appears in monochromatic green picture when the module is lighted. The incidence of this



Fig.4 Vertical line Mura

defect is about 20%, and its distribution on array glass (2.2 m×2.5 m) is irregular.

### 3 Results and Discussions

#### 3.1 Black Hole Defect

The three main steps of the ORG layer are PVX1 DEP, ORG mask and PVX1 etch (also called ORG etch). The difference from other layers is that the organic film here acts as PR (Photoresist), but remains in the array structure without being removed. ORG FICD actually reflects the form after PVX1 etch. It is well known that CuO is black. So the blackening of the hole indicates that the Cu surface inside has been oxidized. In order to clarify the step of Cu oxidation, the pictures obtained before PVX1 deposition and after ORG mask, respectively. Obviously, it can be seen that the position of the base of the hole in Fig. 5 (a) is the same as the SD line. In Fig. 5 (b), all positions except the hole are covered with a layer of PVX1 and ORG, both of which are transparent substances. Therefore, the color of all the locations where the metal is present is the same in DICD (Development Inspection Critical Dimension). Fig. 2 clearly shows that the holes are blackened, illustrating that the defect occurs in PVX1 etch.

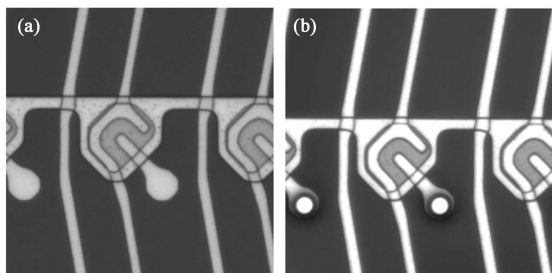


Fig.5 Image of TFT in AA. (a) FICD before PVX1 deposition; (b) DICD after ORG mask.

PVX1 etch uses dry etching to remove about 100 nm of  $\text{SiN}_x$ . Actually this process is divided into two steps. In the first step,  $\text{SF}_6$  and  $\text{O}_2$  with a gas flow ratio of 1 : 2 are used to react with  $\text{SiN}_x$ . As shown in the equation (1), the

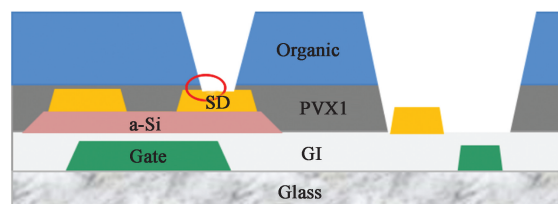
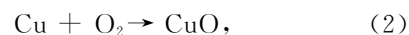


Fig.6 Diagram of CuO protective film

role of  $\text{O}_2$  is to promote the dissociation of  $\text{F}^*$ , from  $\text{SF}_6$  so as to increase the etching rate. In the second step, the gas flow ratio of  $\text{SF}_6$  and  $\text{O}_2$  is changed to 1 : 30. Undercuts of ORG and PVX (as shown in the Fig. 6) are avoided through the reaction between  $\text{O}_2$  and organic film. Unfortunately, during this process, the high content of  $\text{O}_2$  will react with the exposed Cu, resulting in a darker color at the hole shown in the equation (2):



In order to improve this defect, the usual method is to add a gas treatment process.  $\text{H}_2$  is a reducing gas commonly used in factories. After PVX1 etch is completed, array glass is placed in  $\text{H}_2$  plasma (55 500 mL/min) atmosphere for 40 s and then CD is tested. By contrast, it can be seen from Fig. 7 that the hole appears bright white again just like the metal line. Furthermore, the yield of array glass after  $\text{H}_2$  treatment increased by 36%. All these show that  $\text{H}_2$  plasma is effective for reducing CuO and the treatment can improve the contact resistance.

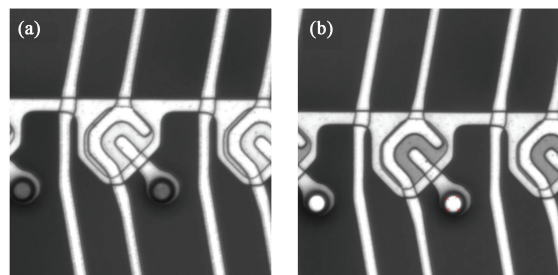


Fig.7 Image of TFT in AA. (a) FICD after PVX1 etch; (b) FICD after  $\text{H}_2$  treatment.

### 3.2 GOA Hole Defect

In order to observe the abnormality of GOA hole, the cross-sectional picture of this area was obtained by SEM (Scanning Electron Microscope) in Fig.8. There is a thick layer of corrosive substance between 2ITO and SD, presumed that SD Cu was reacted. Fig. 9 and Fig. 10 is the picture before 1ITO DEP and after 1ITO etch respectively. According to the pictures, after making 1ITO layer, the surface of SD Cu in GOA area is tightly covered by a layer of corrosion products. While gate Cu remains unchanged because it is covered by GI (Gate Insulator) layer. It can be determined by comparison that the steps of abnormal occurrence is 1ITO layer, which includes 1ITO DEP, 1ITO mask and 1ITO etch. Experience tells us that 1ITO DEP and mask will not cause the deterioration of Cu thin film. Therefore 1ITO etch is the most doubtful step.

1ITO etch includes wet etch and anneal which can convert ITO into a polycrystalline state with low electrical resistance and high transmission rate, so the sample is validated by these two processes separately after 1ITO mask<sup>[5]</sup>. The results show that no abnormality is found in the samples after wet etch. Samples placed in oven at 230 °C for 30 min are shown in Fig. 11(b). There exists a layer of corrosives similar to Fig. 8. This surely serves to illustrate most clearly that the exposed SD Cu will be oxidized by high temperature heating in CDA (Clean dry Air) in anneal process. Thus resulting in the open of GOA circuit.

Attention should be paid to the high temperature environment of Cu when ITO layer is made after SD layer in array process sequence. To solve this problem, we can skip anneal step in 1ITO etch and wait for 2ITO anneal as compensation. In 2ITO anneal, 1ITO or 2ITO covers all the exposed SD Cu, so the oxidation phenomenon caused by anneal will not happen again. On the other hand, when changing design

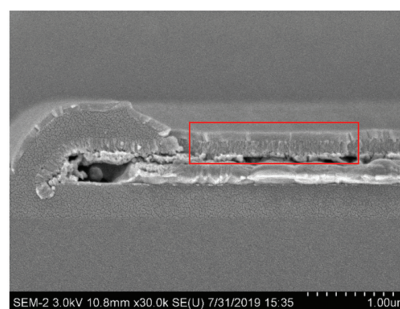


Fig.8 Image of section of the GOA SD hole

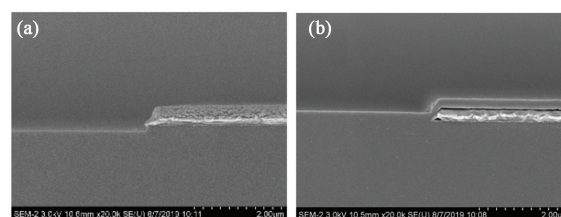


Fig.9 Image of Cu before 1ITO DEP; (a) SD Cu; (b) Gate Cu.

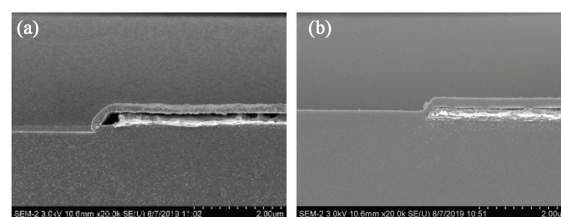


Fig.10 Image of Cu after 1ITO etch. (a) SD Cu; (b) Gate Cu.

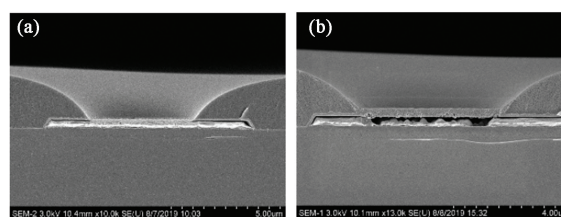


Fig.11 Image of SD Cu in active area. (a) After 1ITO wet etch; (b) After 1ITO anneal.

of 1ITO mask to make all exposed SD Cu covered with PR, the remained 1ITO can protect Cu from oxidation.

### 3.3 Vertical Line Mura

Usually, the abnormal hole will affect the input of electrical signals, resulting in poor qual-

ity of picture<sup>[6]</sup>. In the case of vertical line Mura, gate uses Cu and SD uses Al. The hole in GOA can make the electrical conduction between peripheral circuit and data line of the display area. At the beginning, laser is used to break down the Cu hole to make the electrical conduction there as shown in Fig.12(a). The results show that the breakdown of Cu through gate layer makes the Cu/2ITO lap and Mura disappear. While the crossover hole on SD Al is broken down, the defect remains unchanged. Therefore, it can be judged that the hole on the surface of gate layer is abnormal.

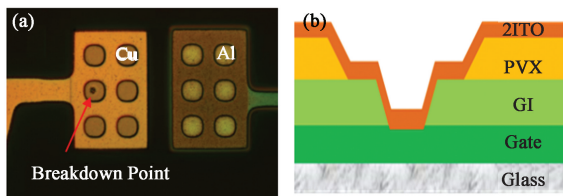


Fig.12 (a) Breakdown of hole by laser in peripheral circuit; (b) Schematic diagram of the section of the gate hole.

Then, the abnormal gate Cu holes are tested by focused ion beam microscopy (FIB). As shown in Fig.13, there is no abnormal 2ITO on the surface of the hole and 2ITO lap at the climbing position with right slope angle. So 2ITO layer is conducting normally. More importantly, the slope angle of the hole is also gentle with no undercut exist. Therefore, it is suspected that the surface corrosion of Cu leads to circuit breakage.

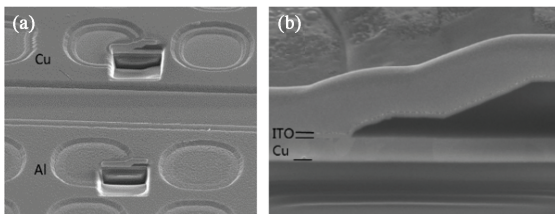


Fig.13 FIB test result of hole. (a) Top view; (b) Cross section of abnormal Cu.

In failure analysis, electrical waveform testing is often used to find defects. Compared with

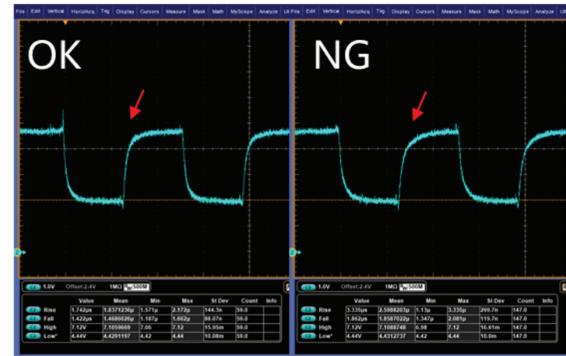


Fig.14 Electrical waveform test of data line

the OK sample from Fig. 14, the NG (Not Good) sample has a delay of  $0.679 \mu\text{s}$  at low voltage and  $0.39 \mu\text{s}$  at high voltage in the rise region of waveform. When the fall part of the waveform is compared with the OK sample, the delay of NG sample is  $0.141 \mu\text{s}$  at low voltage and  $0.137 \mu\text{s}$  at high voltage. In Z-inversion display mode, the data line of monochrome picture fluctuates in each frame<sup>[7]</sup>. Poor contact of data line through the gate holes can cause electric waveform delay in each frame and affect the brightness of the picture. So the vertical line Mura appears in this situation.

VIA etch is dry etch performed using plasma formed of  $\text{SF}_6$  and  $\text{O}_2$ . When the  $\text{O}_2$  content of VIA etch is changed from 62% to 41%, the incidence of vertical line Mura can be reduced to 0%. It can be seen that when the oxygen content in gas of VIA etch is too high, the oxidation reaction of Cu causes the abnormal contact between 2ITO and Cu at the connection hole. The oxidation leads to the increase of data line RC delay and eventually the occurrence of vertical line Mura.

## 4 Conclusion

The oxidation and corrosion of Cu always run through the process of switching from Al material to Cu. Once the Cu thin film is made, every process step in the following must be considered to avoid its reaction with solid, liquid,

gas and plasma. In PVX1 etch, adding  $H_2$  treatment can reduce CuO to Cu and make the hole appear normal color in CD test. If the ITO layer is made after Cu layer, the effect of anneal should be considered. Cu thin film can be protected from oxidation by changing mask design or skipping anneal. In VIA etch, reducing  $O_2$

content of gas can reduce Cu oxidation, thus avoiding the increase of contact resistance. With the diversification of products, the oxidation and corrosion of Cu may appear in a variety of forms. We firmly believe that these defects can be excellently solved by careful researcher.

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